SET UP FOR A FIRST INTEGRATED CIRCUIT CHIP TO ALLOW FOR TESTING OF A CO-PACKAGED SECOND INTEGRATED CIRCUIT CHIP

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ABSTRACT

[0090] A method and system are provided for testing a first integrated circuit chip which is packaged along with at least a second integrated circuit chip in a semiconductor device, wherein at least some external terminals for the semiconductor device are shared by the first and second integrated circuit chips. The method and system include: powering down the second integrated circuit chip; tri-stating a plurality of input/output (I/O) drivers of the second integrated circuit chip so that the plurality of I/O drivers do not drive any signals onto any connections for the shared external terminals; and performing testing of the first integrated circuit chip according to one or more regular testing routines.